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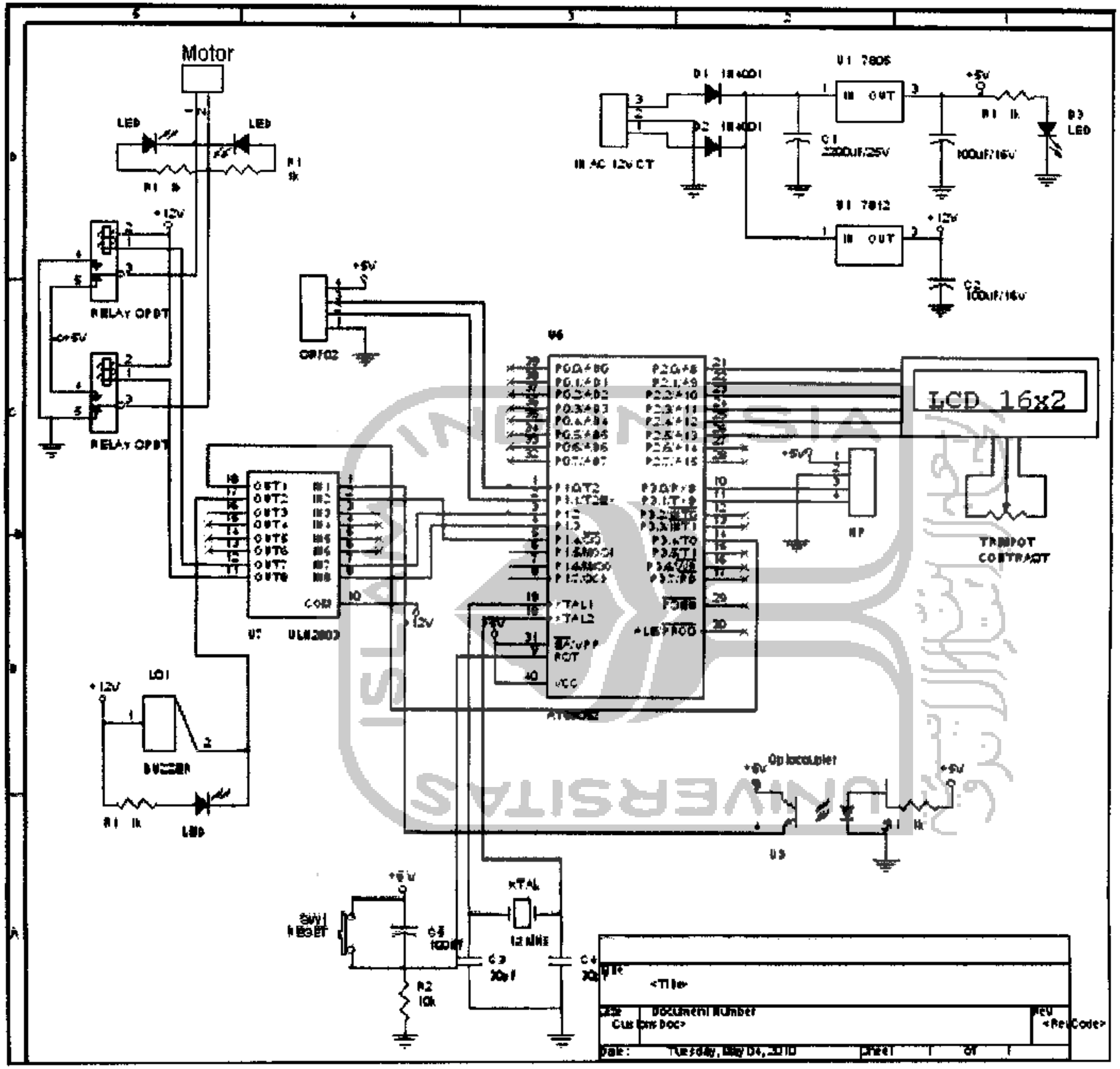
LAMPIRAN

```
$regfile = "8052.dat"
$crystal = 11059200
$baud = 19200
$large

P1 = &B11111011

Config Lcdpin = Pin , Db7 = P2.0 , Db6 = P2.1 , Db5 = P2.2 , Db4 = P2.3 , E = P2.4 , Rs = P2.5
Config Lcd = 16 * 2
Config Timer0 = Counter , Gate = Internal , Mode = 1

Config Scl = P1.0
Config Sda = P1.1

Const Srf02_slaveid = &HE2

Priority Set Timer0
Enable Interrupts
Enable Timer0

Dim C As Byte

Dim Firmware As Byte
Dim I As Byte
Dim Slaveid_read As Byte
Dim Lob As Byte
Dim Hib As Byte
Dim Temp As Byte
Dim Us As Integer
Dim Jarak As Single
Dim Total_jarak As Single
Dim Tinggi As Single
Dim Jaraks As String * 4
Dim Tertutup As Bit
Dim Konter As Byte
Dim Kirimn As Bit , Kirimb As Bit
Dim A As Byte

Alarm Alias P1.4
Slaveid_read = Srf02_slaveid + 1

Gosub Tutup_pintu
Alarm = 0
Cls
Lcd "   PERINGATAN   "
Lowerline
Lcd " BANJIR VIA SMS "
Wait 5

Counter0 = 0
Kirimn = 0
Kirimb = 0
Do
Jarak = 0
Total_jarak = 0
 For I = 1 To 100
```

```
I2cstart
I2cwbyte Srf02_slaveid
I2cwbyte 0
I2cwbyte 82
I2cstop

Ulang:
 Waitms 1
 I2cstart
 I2cwbyte Srf02_slaveid
 I2cwbyte 0
 I2cstop

 I2cstart
 I2cwbyte Slaveid_read
 I2crbyte Firmware , Nack
 I2cstop
 If Firmware = 255 Then Goto Ulang

 I2cstart
 I2cwbyte Srf02_slaveid
 I2cwbyte 2
 I2cstop
 I2cstart
 I2cwbyte Slaveid_read
 I2crbyte Hib , Ack
 I2crbyte Lob , Nack
 Us = Makeint(lob , Hib)

 Jarak = Us * 0.0172
 Total_jarak = Total_jarak + Jarak
Next I

 Jarak = Total_jarak / 100
 Tinggi = 31.5 - Jarak
 Jaraks = Fusing(tinggi , ##.#)
 If Tinggi < 2.5 Then
  Locate 1 , 1
  Lcd "Status: AMAN    "
  Alarm = 0
  Kirimn = 0
  Kirimb = 0
  If Tertutup = 0 Then
   Gosub Tutup_pintu
  End If

 Elseif Tinggi < 3 Then
  Locate 1 , 1
  Lcd "Status: Waspada "
  Alarm = 0
  Kirimb = 0
  If Tertutup = 1 Then
   Gosub Buka_pintu
  End If
  Gosub Sms_naik
```

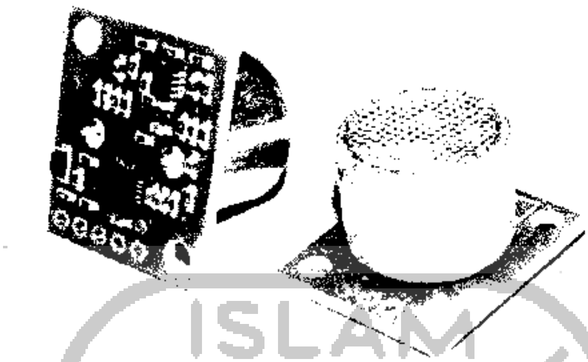
```
 Else
  Locate 1 , 1
  Lcd "Status: BAHAYA! "
  If Tertutup = 1 Then
   Gosub Buka_pintu
  End If
  Gosub Sms_banjir
  Alarm = 1
 End If

 C = 0
 Enable Interrupts
 Counter0 = 0
 Start Counter0
 Wait 1
 Stop Counter0
 Disable Interrupts
 C = Counter0
 Locate 2 , 1
 Lcd "Kec= " ; C ; ", Air= " ; Jaraks

 Waitms 500
Loop

End

Buka_pintu:
 P1.2 = 0
 P1.3 = 0
 Tertutup = 0
 Wait 1
 Gosub Stop_pintu
Return

Tutup_pintu:
 P1.2 = 1
 P1.3 = 1
 Tertutup = 1
 Wait 1
 Gosub Stop_pintu
Return

Stop_pintu:
 P1.2 = 1
 P1.3 = 0
Return

Sms_banjir:
 If Kirimb = 0 Then
  Kirimb = 1
  Cls
  Lcd "Kirim_sms.."
  Waitms 1
  Print "AT+CMGS=24" ; Chr(10) ; Chr(13)
  Wait 1
```

```
 Print "07912658050000F001000D91265847333636F400000BC17B780E1286DDEAB41C" : Chr(26)
 Wait 1
End If
Return

Sms_naik:
If Kirimn = 0 Then
 Kirimn = 1
 Cls
 Lcd "Kirim_sms.."
 Waitms 1
 Print "AT+CMGS=28" ; Chr(10) ; Chr(13)
 Wait 1
 Print "07912658050000F001000D91265847333636F400000FC16B700A0AA7E5207738BD0E8100" ; Chr(26)
 Wait 1
End If
Return
```


Motor
LED
RELAY OPDT
U1 7805
U1 7812
IN AC 12V CT
LCD 16x2
TRIMPOT
CONTRAST
ULN2803
LD1
BUZZER
Optocoupler
XTAL
12 MHz
SW1
RESET
<Title>
Document Number
<RevCode>
Tuesday, May 04, 2010

SRF02 Ultrasonic range finder

Technical Specification



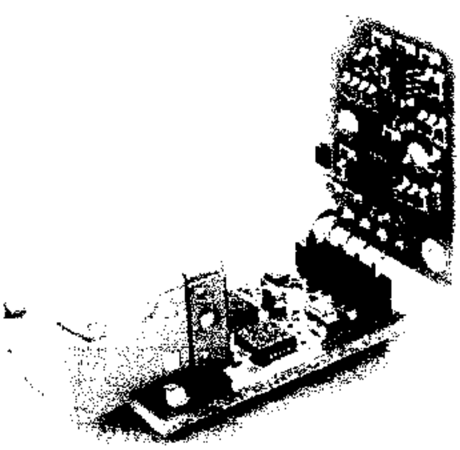
rview

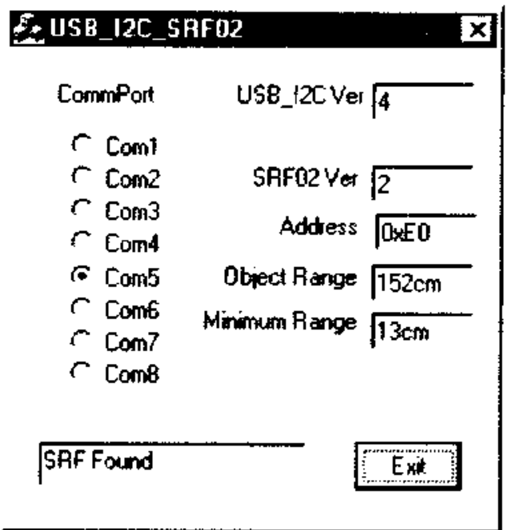
SRF02 is a single transducer ultrasonic rangefinder in a small footprint PCB. It features both and a Serial interfaces. The serial interface is a standard TTL level UART format at 9600 l,1 start, 2 stop and no parity bits, and may be connected directly to the serial ports on any ocontroller. Up to 16 SRF02's may be connected together on a single bus, either I2C or Serial. / commands in the SRF02 include the ability to send an ultrasonic burst on its own without a ption cycle, and the ability to perform a reception cycle without the preceding burst. This has n as requested feature on our sonar's and the SRF02 is the first to see its implementation. ause the SRF02 uses a single transducer for both transmission and reception, the minimum ge is higher than our other dual transducer rangers. The minimum measurement range is around m (6 inches). Like all our rangefinders, the SRF02 can measure in uS, cm or inches.

erating Modes

ere are two operating modes for the SRF02. I2C mode and Serial Mode. This is set with the de pin, connected to 0v Ground for Serial Mode and left unconnected (or tied to +5v Vcc) for : Mode. These are documented on individual pages. For I2C Mode click here, and for Serial de click here.

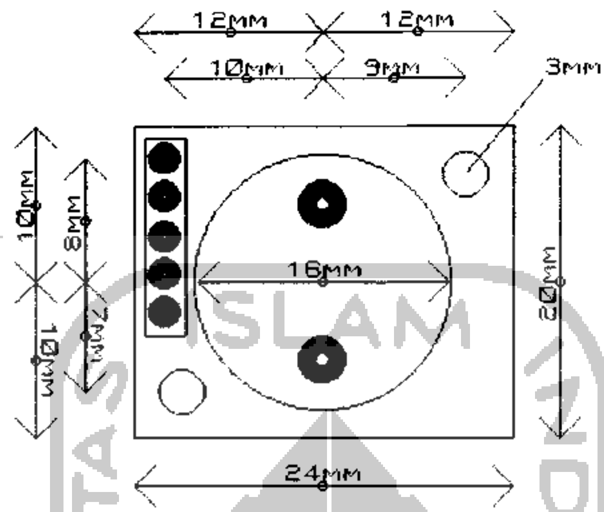
:F02 USB





cting the SRF02 to your PC via USB is this easy. The USBI2C module supplies the SRF02 ower directly from the USB bus. The USB_I2C_SRF02 program can be downloaded here.

nsions



SRF02 Ultrasonic range finder

Technical Specification

I2C Mode

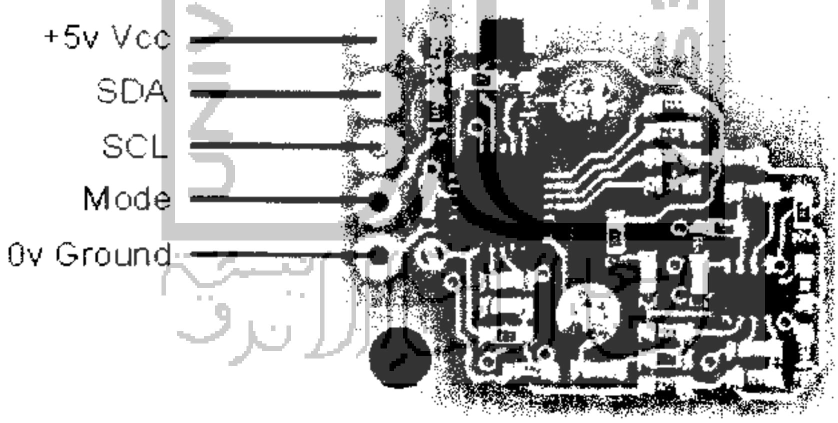
For Serial mode click here

:ommunication

ıe the SRF02 in I2C mode, make sure nothing is connected to the mode pin, it must be left nnected.
.2C bus is available on popular controllers such as the OOPic, Stamp BS2p, PicAxe etc. as as a wide variety of micro-controllers. To the programmer the SRF02 behaves in the same as the ubiquitous 24xx series EEPROM's, except that the I2C address is different. The default ɔed address of the SRF02 is 0xE0. It can be changed by the user to any of 16 addresses E0, Ξ4, E6, E8, EA, EC, EE, F0, F2, F4, F6, F8, FA, FC or FE, therefore up to 16 sonar's can be .

nections

connections to the SRF02 are identical to the SRF08 and SRF10 rangers. The "Mode" pin ıld be left unconnected, it has an internal pull-up resistor. The SCL and SDA lines should each ɜ a pull-up resistor to +5v somewhere on the I2C bus. You only need one pair of resistors, not a for every module. They are normally located with the bus master rather than the slaves. The ᶠ02 is always a slave - never a bus master. If you need them, I recommend 1.8k resistors. Some ɖules such as the OOPic already have pull-up resistors and you do not need to add any more.



egisters

he SRF02 appears as a set of 6 registers.

Location	Read	Write
0	Software Revision	Command Register
1	Unused (reads 0x80)	N/A
2	Range High Byte	N/A
3	Range Low Byte	N/A

4	Autotune Minimum - High Byte	N/A
5	Autotune Minimum - Low Byte	N/A

location 0 can be written to. Location 0 is the command register and is used to start a ranging on. It cannot be read. Reading from location 0 returns the SRF02 software revision. The ng lasts up to 65mS, and the SRF02 will not respond to commands on the I2C bus whilst it is ng.

tions, 2 and 3, are the 16bit unsigned result from the latest ranging - high byte first. The ning of this value depends on the command used, and is either the range in inches, or the range n or the flight time in uS. A value of 0 indicates that no objects were detected. Do not initiate a ing faster than every 65mS to give the previous burst time to fade away.

ations, 4 and 5, are the 16bit unsigned minimum range. This is the approximate closest range sonar can measure to. See the Autotune section below for full details.

nmands

are three commands to initiate a ranging (80 to 82), to return the result in inches, centimeters nicroseconds. Another set of three commands (86 to 88) do the same, but without transmitting burst. These are used where the burst has been transmitted by another sonar. It is up to you to chronize the commands to the two sonar's. There is a command (92) to transmit a burst without ng the ranging and also a set of commands to change the I2C address.

Command		Action
Decimal	Hex	
80	0x50	Real Ranging Mode - Result in inches
81	0x51	Real Ranging Mode - Result in centimeters
82	0x52	Real Ranging Mode - Result in micro-seconds
86	0x56	Fake Ranging Mode - Result in inches
87	0x57	Fake Ranging Mode - Result in centimeters
88	0x58	Fake Ranging Mode - Result in micro-seconds
92	0x5C	Transmit an 8 cycle 40khz burst - no ranging takes place
96	0x60	Force Autotune Restart - same as power-up. You can ignore this command.
160	0xA0	1st in sequence to change I2C address
165	0xA5	3rd in sequence to change I2C address
170	0xAA	2nd in sequence to change I2C address

FA	1
FC	1
FE	1

ng

iate a ranging, write one of the above commands to the command register and wait the ed amount of time for completion and read the result. The echo buffer is cleared at the start h ranging. The ranging lasts up to 66mS, after this the range can be read from locations 2

king for Completion of Ranging

o not have to use a timer on your own controller to wait for ranging to finish. You can take itage of the fact that the SRF02 will not respond to any I2C activity whilst ranging. fore, if you try to read from the SRF02 (we use the software revision number a location 0) you will get 255 (0xFF) whilst ranging. This is because the I2C data line (SDA) is pulled if nothing is driving it. As soon as the ranging is complete the SRF02 will again respond to 2C bus, so just keep reading the register until its not 255 (0xFF) anymore. You can then read onar data. Your controller can take advantage of this to perform other tasks while the SRF02 iging. The SRF02 will always be ready 70mS after initiating the ranging.

red LED is used to flash out a code for the I2C address on power-up (see below). It also gives ef flash during the "ping" whilst ranging.

nging the I2C Bus Address

hange the I2C address of the SRF02 you must have only one sonar on the bus. Write the 3 ence commands in the correct order followed by the address. Example; to change the address sonar currently at 0xE0 (the default shipped address) to 0xF2, write the following to address 0; (0xA0, 0xAA, 0xA5, 0xF2). These commands must be sent in the correct sequence to nge the I2C address, additionally, No other command may be issued in the middle of the uence. The sequence must be sent to the command register at location 0, which means 4 arate write transactions on the I2C bus. When done, you should label the sonar with its address, vever if you do forget, just power it up without sending any commands. The SRF02 will flash address out on the LED. One long flash followed by a number of shorter flashes indicating its lress. The flashing is terminated immediately on sending a command the SRF02.

Address		Long Flash	Short flashes
Decimal	Hex		
224	E0	1	0
226	E2	1	1
228	E4	1	2
230	E6	1	3
232	E8	1	4
234	EA	1	5
236	EC	1	6
238	EE	1	7
240	F0	1	8
242	F2	1	9
244	F4	1	10
246	F6	1	11
248	F8	1	12

r to the same a
s stored in the
0xEC, 0xEE,
x06, 0x07, 0x0
alibration. Yo
ening automat
cer keeps on r
02 can measu
is normally th
RF02 is able t
g the SRF02
m (11"). The
n 5-6 rangin
continue to
g it out a bit
vith no impac
required by
as the range
nore this co

SRF02 Ultrasonic range finder

Technical Specification

Serial Mode

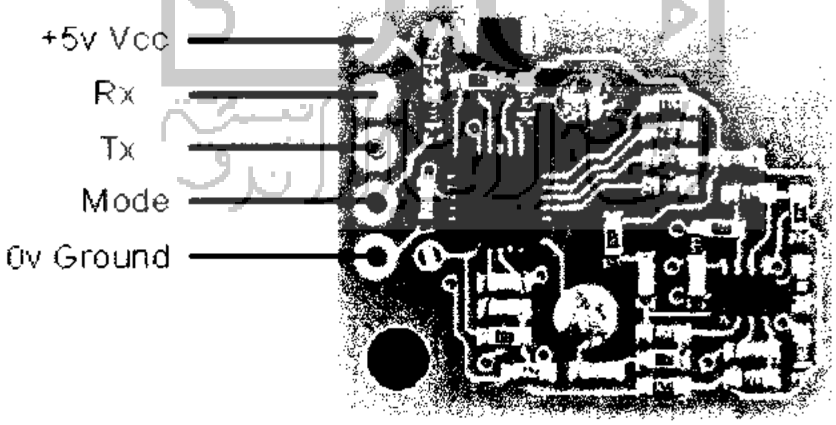
For I2C mode click here

| Communication

; the SRF02 in Serial mode, make sure the Mode pin is connected to 0v Ground.
data is fixed at 9600 baud 1 start, 2 stop and no parity bits. Serial data is a TTL level signal - IOT RS232. Do not connect the SRF02 to an RS232 port - you will destroy the module! If /ould like to connect the SRF02 to your PC's RS232 port, you must use a MAX232 or similar e. It can also be used (in I2C mode) with the USBI2C module to make a self powered USB :r, see the examples page for details. Many small controllers such as the OOPic, Stamp BS2p, xe etc. as well as a wide variety of micro-controllers have serial ports. To communicate with RF02, you simply need to send two bytes, the address of the SRF02 (factory default is 0) and ommand. The default shipped address can be changed by the user to any of 16 addresses 0, 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, or 15, therefore up to 16 sonar's can be used.

nections

connections to the SRF02 are shown below. The "Mode" pin must be connected to 0v ground ace the SRF02 in serial mode. The Rx pin is data into the SRF02 and should be connected to Tx pin on your controller. The Tx pin is data out of the SRF02 and should be connected to the ɔin on your controller. If you're using multiple SRF02's, you can connect them all up to the e serial port on your controller. Connect the Tx from your controller to all the Rx pins on the F02's and connect the Rx pin on your controller to all the Tx pins on the SRF02's. This works ause the Tx pins are high impedance (just a weak pull-up to 5v), except when actually sending ı. Just make sure all the SRF02's are programmed to different addresses.



ommands

ɔ send a command to the SRF02, you need to send two bytes. The first is the SRF02's address 0 15, (0x00 to 0x0F) and then the actual command itself - see below. The are three commands to itiate a ranging (80 to 82), to produce the result in inches, centimeters or microseconds. These ıree commands don't Tx the result back to your controller. You should wait 70mS and then use ɔmmand 94 to get the result of the ranging. Another set of three commands (83 to 85) do the ıme, but also transmits the result of the ranging back to your controller as soon as it is available. ogether, these six commands (80 - 85) are called "Real" because they perform a complete ınging. There is another set of six commands (86 - 91) called "Fake". They are the same as the

commands except that they do not send the 8-cycle burst out. These are used where the
ıas been transmitted by another sonar. It is up to you to synchronize the commands to the
ınar's. There is a command (92) to transmit a burst without doing the ranging.
ıand 93 is used to get the firmware revision of the SRF02.
ıand 94 gets returns two bytes (high byte first) from the most recent ranging. Put them
er to make a 16-bit result.
ıands 95 and 96 are used by the Autotune algorithms - See the Autotune section below for
s.

Command		Action
ecimal	Hex	
80	0x50	Real Ranging Mode - Result in inches
81	0x51	Real Ranging Mode - Result in centimeters
82	0x52	Real Ranging Mode - Result in micro-seconds
83	0x53	Real Ranging Mode - Result in inches, automatically Tx range back to controller as soon as ranging is complete.
84	0x54	Real Ranging Mode - Result in centimeters, automatically Tx range back to controller as soon as ranging is complete.
85	0x55	Real Ranging Mode - Result in micro-seconds, automatically Tx range back to controller as soon as ranging is complete.
86	0x56	Fake Ranging Mode - Result in inches
87	0x57	Fake Ranging Mode - Result in centimeters
88	0x58	Fake Ranging Mode - Result in micro-seconds
89	0x59	Fake Ranging Mode - Result in inches, automatically Tx range back to controller as soon as ranging is complete.
90	0x5A	Fake Ranging Mode - Result in centimeters, automatically Tx range back to controller as soon as ranging is complete.
91	0x5B	Fake Ranging Mode - Result in micro-seconds, automatically Tx range back to controller as soon as ranging is complete.
92	0x5C	Transmit an 8 cycle 40khz burst - no ranging takes place
93	0x5D	Get software version - sends a single byte back to the controller
94	0x5E	Get Range, returns two bytes (high byte first) from the most recent ranging.
95	0x5F	Get Minimum, returns two bytes (high byte first) of the closest range measurable - see Autotune section
96	0x60	Force Autotune Restart - same as power-up. You can ignore this command.
160	0xA0	1st in sequence to change I2C address
165	0xA5	3rd in sequence to change I2C address
170	0xAA	2nd in sequence to change I2C address

ED

he red LED is used to flash out a code for the I2C address on power-up (see below). It also gives flash during the "ping" whilst ranging.

ging the SRF02 Address
inge the address of the SRF02 you must have only one sonar connected. Write the 3 ice commands in the correct order followed by the address. Example; to change the address onar currently at 0 (the default shipped address) to 5, write the following to address 0; (0xA0, , 0xA5, 0x05). These commands must be sent in the correct sequence to change the I2C ss, additionally, No other command may be issued in the middle of the sequence. The nce must be sent as four separate commands to the current address of the sonar. i.e. 0x00, then 0x00, 0xAA, then 0x00, 0xA5 and finally 0x00, 0x05. When done, you should label the with its new address, however if you do forget, just power it up without sending any nands. The SRF02 will flash its address out on the LED. One long flash followed by a er of shorter flashes indicating its address. The flashing is terminated immediately on sending nmand the SRF02.

Address		Long Flash	Short flashes
Decimal	Hex		
0	00	1	0
1	01	1	1
2	02	1	2
3	03	1	3
4	04	1	4
5	05	1	5
6	06	1	6
7	07	1	7
8	08	1	8
9	09	1	9
10	0A	1	10
11	0B	1	11
12	0C	1	12
13	0D	1	13
14	0E	1	14
15	0F	1	15

ke care not to set more than one sonar to the same address, there will be a bus collision and very predictable results.

ote - there is only one module address stored in the SRF02. If you change it, the equivalent I2C ldress will also change:
x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, x0F Serial addresses
xE0, 0xE2, 0xE4, 0xE6, 0xE8, 0xEA, 0xEC, 0xEE, 0xF0, 0xF2, 0xF4, 0xF6, 0xF8, 0xFA, 0xFC, xFE Equivalent I2C addresses

utoTune
he SRF02 does not require any user calibration. You power up and go right ahead and use the RF02.

ılly, there are tuning cycles happening automatically in the background. After the ultrasonic ıas been transmitted, the transducer keeps on ringing for a period of time. It is this ringing limits the closest range the SRF02 can measure. This time period varies with temperature ɔm transducer to transducer, but is normally the equivalent of 11 to 16cm (4" to 6"), a bit f the transducer is warm. The SRF02 is able to detect the transducer ring time and move its ion threshold right up to it, giving the SRF02 the very best performance possible. On power e detection threshold is set to 28cm (11"). The tuning algorithms quickly back this right up to ınsducer ring. This happens within 5-6 ranging cycles - less than half a second at full scan . After this the tuning algorithms continue to monitor the transducer, backing the threshold en further when possible or easing it out a bit when necessary. The tuning algorithms work ıatically, in the background and with no impact on scan time.

ninimum range can be checked, if required by sending command 95. This will return the st measurable range in uS, cm or inches, the same as the range. It is also possible to make the 02 re-tune by writing command 96 but you can ignore this command. It is used during our ıg.

'Products
ogrammable (ISP) Flash Memory
te/Erase Cycles
nge
Hz to 33 MHz
nory Lock

Channel
er-down Modes
Power-down Mode

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

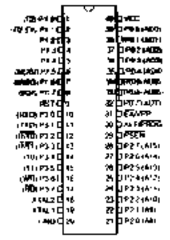
AT89S52

ower, high-performance CMOS 8-bit microcontroller with 8K ammable Flash memory The device is manufactured using volatile memory technology and is compatible with the indus- uction set and pinout The on-chip Flash allows the program amed in-system or by a conventional nonvolatile memory pro- a versatile 8-bit CPU with in-system programmable Flash on tmel AT89S52 is a powerful microcontroller which provides a effective solution to many embedded control applications

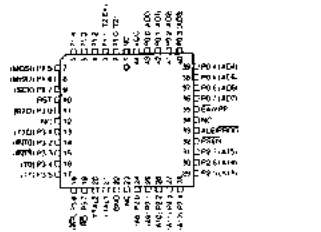
the following standard features. 8K bytes of Flash, 256 bytes atchdog timer, two data pointers, three 16-bit timer/counters a errupt architecture, a full duplex serial port, on-chip oscillator, ddition, the AT89S52 is designed with static logic for operation and supports two software selectable power saving modes CPU while allowing the RAM, timer/counters, serial port, and inue functioning The Power-down mode saves the RAM con- cillator, disabling all other chip functions until the next interrupt

Pin Configurations

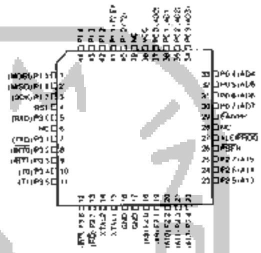
PDIP

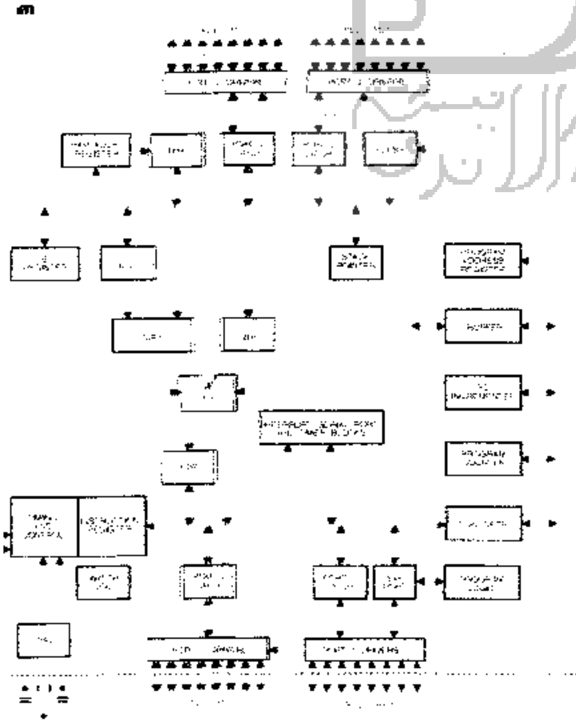


PLCC



TQFP





Pin Description

VCC
Supply voltage

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table

Port 1 also receives the low-order address bytes during Flash programming and verification

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2) clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups The Port 2 output buffers can sink/source four TTL inputs When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups The Port 3 output buffers can sink/source four TTL inputs When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups

Port 3 also serves the functions of various special features of the AT89S52 as shown in the following table

Port 3 also receives some control signals for Flash programming and verification

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled

ALE/$\overline{PROG}$
Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is

ng the ALE-disable bit has no
is in external execution mode

$\overline{\text{PSEN}}$) is the read strobe to exter-

ecuting code from external pro-
activated twice each machine
$\overline{\text{N}}$ activations are skipped during
ata memory

$\overline{\text{EA}}$ must be strapped to GND in
: to fetch code from external pro
starting at 0000H up to FFFFH

Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit

XTAL2

Output from the inverting oscillator amplifier

Map and Reset Values

							0FFH
							0F7H
							0EFH
							0E7H
							0DFH
							0D7H
T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
							0C7H
							0BFH
							0B7H
							0AFH
	AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
SBUF XXXXXXXX							9FH
							97H
TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Special Function Registers

A map of the on chip memory area called the Special Function Register (SFR) space is shown in Table 1

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2 The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register Two priorities can be set for each of the six interrupt sources in the IP register

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software TF2 will not be set when either RCLK = 1 or TCLK = 1
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1 When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine EXF2 must be cleared by software EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3 RCLK = 0 causes Timer 1 overflow to be used for the receive clock
TCLK	Transmit clock enable When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3 TCLK = 0 causes Timer 1 overflows to be used for the transmit clock
EXEN2	Timer 2 external enable When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port EXEN2 = 0 causes Timer 2 to ignore events at T2EX
TR2	Start/Stop control for Timer 2 TR2 = 1 starts the timer
$C/\overline{T2}$	Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function $C/\overline{T2}$ = 1 for external event counter (falling edge triggered)
$CP/\overline{RL2}$	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1 $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1 When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

uxiliary Register

ddress = 8EH — Reset Value = XXX00XX0B

ot Bit Addressable

Bit	–	–	–	WDIDLE	DISRTO	–		DISALE
	7	6	5	4	3	2	1	0

ved for future expansion

le/Enable ALE

LE Operating Mode

ALE is emitted at a constant rate of 1/6 the oscillator frequency

ALE is active only during a MOVX or MOVC instruction

le/Enable Reset out

RTO

Reset pin is driven High after WDT times out

Reset pin is input only

ble/Enable WDT in IDLE mode

DLE

WDT continues to count in IDLE mode

WDT halts counting in IDLE mode

er Registers: To facilitate accessing both ernal data memory, two banks of 16-bit gisters are provided DP0 at SFR address 83H and DP1 at 84H 85H Bit DPS = 0 selects DP0 and DPS = 1 selects DP1 ld always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON 4) in the PCON SFR POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

1 Auxiliary Register 1

Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	–	–	–	–	–	–	–	DPS
	7	6	5	4	3	2	1	0

served for future expansion

ta Pointer Register Select

PS

Selects DPTR Registers DP0L, DP0H

Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory Up to 64K bytes each of external Program and Data Memory can be addressed

Program Memory

If the $\overline{\text{EA}}$ pin is connected to GND, all program fetches are directed to external memory

On the AT89S52, if $\overline{\text{EA}}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM The upper 128 bytes occupy a parallel address space to the Special Function Registers This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2)

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM For example, the following indirect addressing instruction, where R0 contains 0A0H accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H)

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space

...l with Reset-out)

...recovery method in situations ...bjected to software upsets. The ...ounter and the Watchdog Timer ...ne WDT is defaulted to disable ...ble the WDT, a user must write ...ence to the WDTRST register ...en the WDT is enabled, it will ...cycle while the oscillator is run- ...nod is dependent on the external ...is no way to disable the WDT ...a hardware reset or WDT over- ...verflows, it will drive an output ...RST pin.

...er must write 01EH and 0E1H in ...l register (SFR location 0A6H) ...d, the user needs to service it by ...WDTRST to avoid a WDT over ...overflows when it reaches 8191 ...set the device. When the WDT is ...t every machine cycle while the ...s means the user must reset the ...1 machine cycles. To reset the ...e 01EH and 0E1H to WDTRST ...egister. The WDT counter cannot ...WDT overflows, it will generate an ...the RST pin. The RESET pulse ...ere TOSC=1/FOSC. To make the ...should be serviced in those sec ...eriodically be executed within the ...a WDT reset.

...ver-down and Idle

...e oscillator stops, which means the ...e in Power-down mode, the user ...a the WDT. There are two methods ...node: by a hardware reset or via a ...interrupt which is enabled prior to ...node. When Power-down is exited ...rvicing the WDT should occur as it ...ver the AT89S52 is reset. Exiting ...terrupt is significantly different. The ...g enough for the oscillator to stabi- ...pt is brought high, the interrupt is ...he WDT from resetting the device ...is held low, the WDT is not started ...ulled high. It is suggested that the ...the interrupt service for the interrupt ...wn mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 5. Timer in Capture Mode

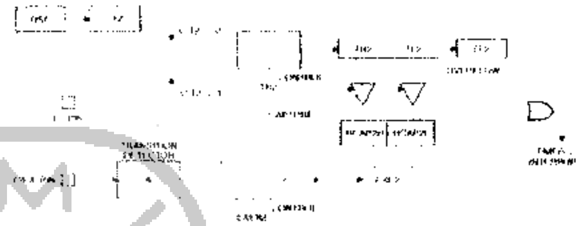


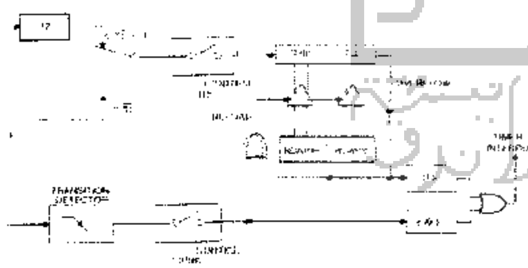
Figure 6 shows Timer 2 automatically counting up when DCEN=0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

...uto Reload Mode (DCEN = 0)



Timer 2 Mode Control Register

...ss = 0C9H — Reset Value = XXXX XX00B

...sable

–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

	Function
	Not implemented, reserved for future
	Timer 2 Output Enable bit
	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 7. Timer 2 Auto Reload Mode (DCEN = 1)

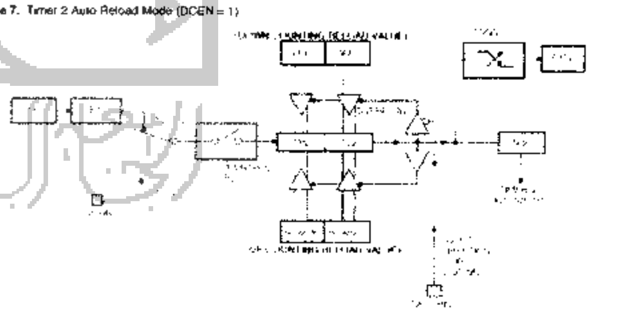
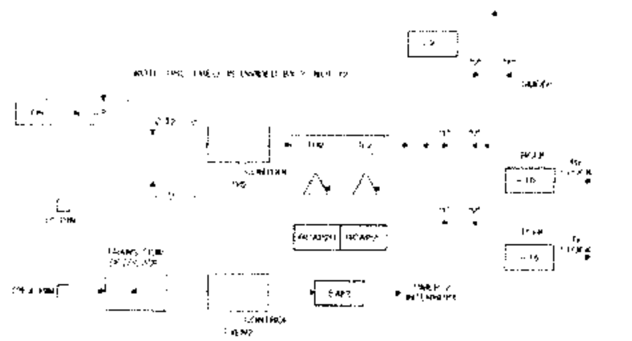


Figure 8. Timer 2 in Baud Rate Generator Mode



ator

e baud rate generator by setting 2CON (Table 2) Note that the d receive can be different if Timer or transmitter and Timer 1 is used etting RCLK and/or TCLK puts generator mode, as shown in Fig-

mode is similar to the auto-reload TH2 causes the Timer 2 registers 6-bit value in registers RCAP2H preset by software.

1 and 3 are determined by Timer g to the following equation

lates $\frac{\text{Timer 2 Overflow Rate}}{16}$

gured for either timer or counter cations, it is configured for timer The timer operation is different for as a baud rate generator Normally, s every machine cycle (at 1/12 the , a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency) The baud rate formula is given below

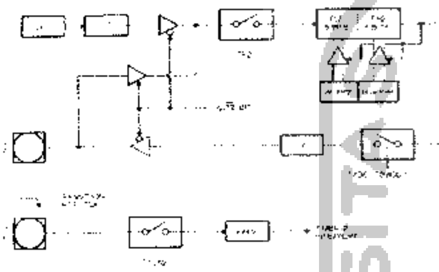
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536-(RCAP2H,RCAP2L)]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer

Timer 2 as a baud rate generator is shown in Figure 8 This figure is valid only if RCLK or TCLK = 1 in T2CON Note that a rollover in TH2 does not set TF2 and will not generate an interrupt Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2) Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers

ock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 9 This pin, besides being a regular I/O pin has two alternate functions It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON 1) must be cleared and bit T2OE (T2MOD 1) must be set Bit TR2 (T2CON 2) starts and stops the timer

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(RCAP2H,RCAP2L)]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt This behavior is similar to when Timer 2 is used as a baud-rate generator It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L

Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt These interrupts are all shown in Figure 10

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented In the AT89S52, bit position IE.5 is also unimplemented User software should not write 1s to these bit positions, since they may be used in future AT89 products

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON Neither of these flags is cleared by hardware when the service routine is vectored to In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow The values are then polled by the circuitry in the next cycle However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

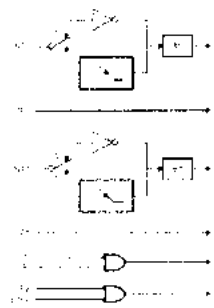
(MSB)							(LSB)
EA		ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt

Symbol	Position	Function
EA	IE 7	Disables all interrupts If EA = 0 no interrupt is acknowledged If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit
–	IE 6	Reserved
ET2	IE 5	Timer 2 interrupt enable bit
ES	IE 4	Serial Port interrupt enable bit
ET1	IE 3	Timer 1 interrupt enable bit
EX1	IE 2	External interrupt 1 enable bit
ET0	IE 1	Timer 0 interrupt enable bit
EX0	IE 0	External interrupt 0 enable bit
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products		

Figure 10. Interrupt Sources



haracteristics

are the input and output, respectively, plifier that can be configured for use as or, as shown in Figure 11 Either a quartz resonator may be used To drive the ernal clock source, XTAL2 should be left XTAL1 is driven, as shown in Figure 12. rements on the duty cycle of the external the input to the internal clocking circuitry by two flip-flop, but minimum and maximum h and low time specifications must be

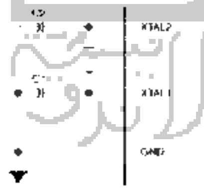
CPU puts itself to sleep while all the on- remain active The mode is invoked by ntent of the on-chip RAM and all the spe gisters remain unchanged during this node can be terminated by any enabled hardware reset.

idle mode is terminated by a hardware e normally resumes program execution off, up to two machine cycles before the gorithm takes control. On-chip hardware internal RAM in this event, but access to not inhibited. To eliminate the possibility of write to a port pin when idle mode is termi- t, the instruction following the one that le should not write to a port pin or to exter-

n Mode

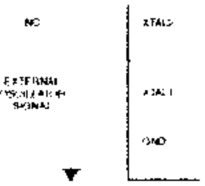
wn mode, the oscillator is stopped, and the invokes Power-down is the last instruction on-chip RAM and Special Function Regs values until the Power-down mode is termi- Power down mode can be initiated either reset or by an enabled external interrupt the SFRs but does not change the on-chip et should not be activated before V_{CC} is normal operating level and must be held active long enough to allow the oscillator to restart and stabilize

Figure 11. Oscillator Connections



Note C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



s of External Pins During Idle and Power-down Modes

Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Internal	1	1	Data	Data	Data	Data
External	1	1	Float	Data	Address	Data
Internal	0	0	Data	Data	Data	Data
External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table

Table 7. Lock Bit Protection Modes

Program Lock Bits	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly

Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers

The AT89S52 code memory array is programmed byte-by-byte

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14 To program the AT89S52, take the following steps

1 Input the desired memory location on the address lines
2 Input the appropriate data byte on the data lines
3 Activate the correct combination of control signals
4 Raise $\overline{EA}/V_{PP}$ to 12V
5 Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits The byte-write cycle is self-timed and typically takes no more than 50 µs.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0 7 Once the write cycle has been completed true data is valid on all outputs, and the next cycle may begin $\overline{Data}$ Polling may begin any time after a write cycle has been initiated

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$ P3.0 is pulled high again when programming is done to indicate READY

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification The status of the individual lock bits can be verified directly by reading them back

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3 6 and P3 7 must be pulled to a logic low The values returned are as follows

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction In this mode, chip erase is self-timed and takes about 500 ms

During chip erase, a serial read from any address location will return 00H at the data output

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output) After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed Before a reprogramming sequence can occur, a Chip Erase operation is required

The Chip Erase operation turns the content of every memory location in the Code array into FFH

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2 The maximum serial clock (SCK) s than 1/16 of the crystal fre- ... cillator clock, the maximum SCK

Algorithm

AT89S52 in the serial program- ... sequence is recommended

VCC and GND pins

nnected across pins XTAL1 and ... lz to 33 MHz clock to XTAL1 pin ... 0 milliseconds

nming by sending the Pro- ... ial instruction to pin ... uency of the shift clock sup- ... needs to be less than the ... divided by 16

ogrammed one byte at a time ... ess and data together with the appropriate Write Instruction. The write cycle is self-timed and typically takes less than 1 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used)
Set RST to "L"
Turn V_{CC} power off

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 8. Flash Programming Modes

Mode	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 13. Programming the Flash Memory (Parallel Mode)

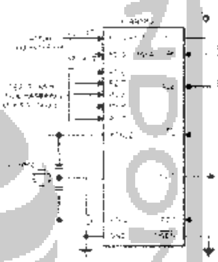
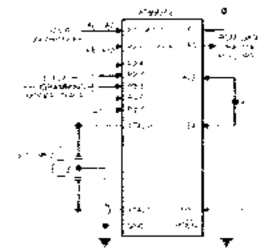


Figure 14. Verifying the Flash Memory (Parallel Mode)



...mming and Verification Characteristics (Parallel Mode)

V_{CC} = 4.5 to 5.5V

Parameter	Min	Max	Units
Programming Supply Voltage	11.5	12.5	V
Programming Supply Current		10	mA
V_{CC} Supply Current		30	mA
Oscillator Frequency	3	33	MHz
Address Setup to PROG Low	$48t_{CLCL}$		
Address Hold After PROG	$48t_{CLCL}$		
Data Setup to PROG Low	$48t_{CLCL}$		
Data Hold After PROG	$48t_{CLCL}$		
P2.7 (ENABLE) High to V_{PP}	$48t_{CLCL}$		
V_{PP} Setup to PROG Low	10		µs
V_{PP} Hold After PROG	10		µs
PROG Width	0.2	1	µs
Address to Data Valid		$48t_{CLCL}$	
ENABLE Low to Data Valid		$48t_{CLCL}$	
Data Float After ENABLE	0	$48t_{CLCL}$	
PROG High to BUSY Low		1.0	µs
Byte Write Cycle Time		50	µs

... Programming and Verification Waveforms – Parallel Mode

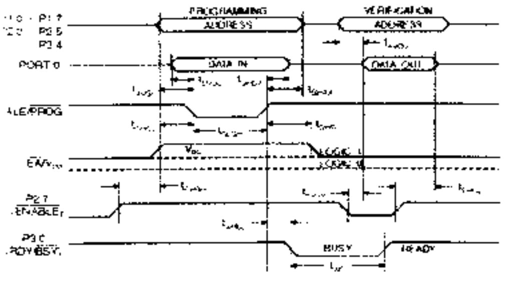
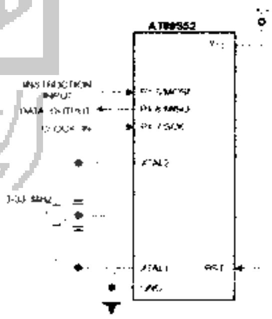
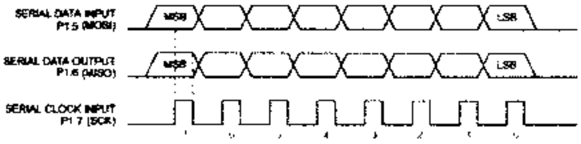


Figure 16. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 17. Serial Programming Waveforms



ng Instruction Set

Instruction Format				
Byte 1	Byte 2	Byte 3	Byte 4	Operation
010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
010 0000	xxx [illegible]	[illegible]	[illegible]	Read data from Program memory in the byte mode
100 0000	xxx [illegible]	[illegible]	[illegible]	Write data to Program memory in the byte mode
010 1100	1110 00 [illegible]	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
0010 0100	xxxx xxxx	xxxx xxxx	[illegible] xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
0010 1000	xxx [illegible]	xxx xxxx	Signature Byte	Read Signature Byte
0011 0000	xxx [illegible]	Byte 0	Byte 1 ... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
0101 0000	xxx [illegible]	Byte 0	Byte 1 ... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

bytes are not readable in Lock Bit Modes 3 and 4

---> Mode 1, no lock protection
---> Mode 2, lock bit 1 activated
---> Mode 3, lock bit 2 activated
---> Mode 4, lock bit 3 activated

Each of the lock bits needs to be activated sequentially before Mode 4 can be executed

, SCK should be low for at least 64 goes high to clock in the enable of Reset signal is necessary. SCK than 1/16 of the system clock at

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

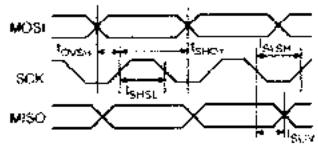


Figure 18. Serial Programming Timing

Table 10. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$2 t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$2 t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2 t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64 t_{CLCL} + 400$	μs

ximum Ratings*

ure	-55°C to +125°C
e	-65°C to +150°C
und	-1.0V to +7.0V
g Voltage	6.6V
	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

eristics

in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted

rameter	Condition	Min	Max	Units
put Low Voltage	(Except $\overline{EA}$)	-0.5	$0.2 V_{CC}$-0.1	V
put Low Voltage ($\overline{EA}$)		-0.5	$0.2 V_{CC}$-0.3	V
put High Voltage	(Except XTAL1, RST)	$0.2 V_{CC}$+0.9	V_{CC}+0.5	V
put High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	V_{CC}+0.5	V
tput Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
tput Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 μA, V_{CC} = 5V ± 10%	2.4		V
	I_{OH} = -25 μA	$0.75 V_{CC}$		V
	I_{OH} = -10 μA	$0.9 V_{CC}$		V
Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 μA, V_{CC} = 5V ± 10%	2.4		V
	I_{OH} = -300 μA	$0.75 V_{CC}$		V
	I_{OH} = -80 μA	$0.9 V_{CC}$		V
Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V	-50		μA
Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	μA
Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
Reset Pulldown Resistor		10	30	KΩ
Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
Power Supply Current	Active Mode, 12 MHz		25	mA
	Idle Mode, 12 MHz		6.5	mA
Power-down Mode[1]	V_{CC} = 5.5V		50	μA

er steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
imum I_{OL} per port pin: 10 mA
imum I_{OL} per 8-bit port:
0: 26 mA Ports 1, 2, 3: 15 mA
imum total I_{OL} for all output pins: 71 mA
$_{L}$ exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater the listed test conditions.
imum V_{CC} for Power-down is 2V

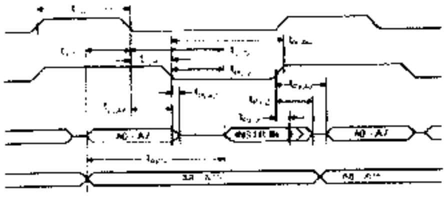
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

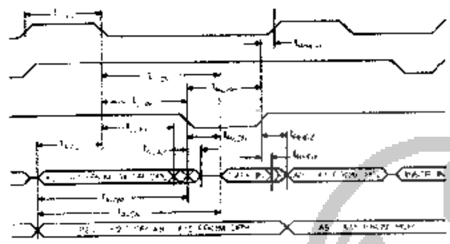
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

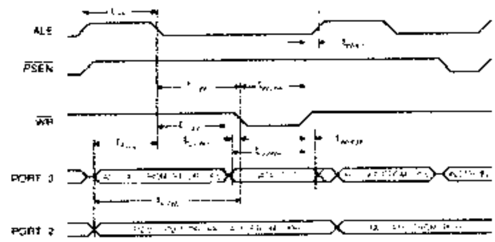
Memory Read Cycle



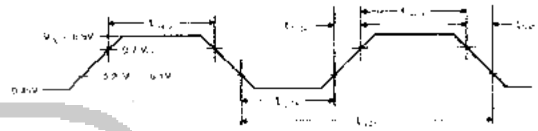
mory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

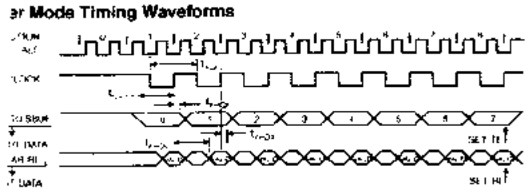
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

ming: Shift Register Mode Test Conditions

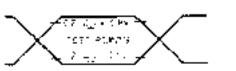
able are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF

	12 MHz Osc		Variable Oscillator		
meter	Min	Max	Min	Max	Units
k Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
out Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
out Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t Data Hold After Clock Rising Edge	0		0		ns
k Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

er Mode Timing Waveforms



Input/Output Waveforms[1]



nputs during testing are driven at V_{CC} - 0.5V logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} for a logic 0.

Float Waveforms[1]

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC	44A	Commercial (0°C to 70°C)
		AT89S52-24JC	44J	
		AT89S52-24PC	40P6	
		AT89S52-24AI	44A	Industrial (-40°C to 85°C)
		AT89S52-24JI	44J	
		AT89S52-24PI	40P6	
33	4.5V to 5.5V	AT89S52-33AC	44A	Commercial (0°C to 70°C)
		AT89S52-33JC	44J	
		AT89S52-33PC	40P6	

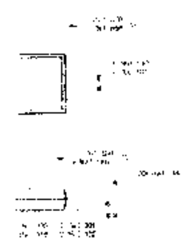
- Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

ıtion

mm) Plastic Gull Wing Quad

rs and (Inches)*



n millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC) Dimensions in Inches and (Millimeters)

Wide, Plastic Dual Inline

s and (Millimeters)

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44306 Nantes Cedex 3, France
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FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

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Rev. 1919A–07/01/MM

nformation

…ation, the manual reference to the AT command set supported by S45 Siemens

…tions and glossary

…viations and terms are used throughout this specification

…m	Meaning
	Acronym for " Fixed dialing numbers "
	Packet Data Unit
	Acronym for "Personal Identification Number"
	Acronym for "PIN Unblocking Key "

…al Conventions

…tional conventions apply throughout this manual.
…ts in Courier New indicate parameter names and values

…nts indicate the default value of the parameter at hand

…("") are used to indicate text strings

…er) inside quotes are interpreted as text strings

…are not included in double quotes must be separated by comma

…strings are ignored unless they are included in double quotes

…ns applying to the presentation of AT commands are outlined in section 2.2

…onventions

…er conventions apply throughout this manual.
…es in strings can be omitted

…parameter (<value>) is omitted in V.25ter commands, the value 0 is assumed

…names of commands are not case-sensitive, cases should not be mixed. Either "AT" or "at" …ecified, but neither "aT" nor "At

…d documentation

…sted in this section are related to the current document

… Siemens-internal documentation

…nal documents are related to the current document

1.6.2 Related Standardisation documentation

The following standardisation documents are related to the current document

[1] Digital cellular telecommunications system (Phase 2+) AT command set for GSM Mobile Equipment (ME) (GSM 07.07 version 6.4.0 Release 1997)
Reference No [illegible]

[2] Digital cellular telecommunications system (Phase 2+) Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (GSM 07.05 version 6.0.0 Release 1997)
Reference No [illegible]

[3] ITU-T Draft new Recommendation V.25ter "Serial asynchronous automatic dialling and control"

[4] "Digital cellular telecommunication system (Phase 2+). Personalisation of GSM Mobile Equipment (ME) Mobile functionality specification" (GSM 02.22)

[5] "Digital cellular telecommunication system (Phase 2+). Specification of the Subscriber Identification Module - Mobile Equipment (SIM-ME) interface" (GSM 11.11)

[6] "Facsimile Digital Interfaces - Asynchronous Facsimile DCE Control Standard, Service Class 1(TIA/EIA-578-A), May 1995

[7] Standards Proposal No. 2388, Proposed New Standard "Asynchronous Facsimile DCE Control Standard" (if approved, to be published as EIA/TIA-592), October 1990

GSM04.11
GSM03.40

1.6.3 Change Requests related to the feature

The following new change requests are taken into account in this document: none

…ware interface

…rview of the supported AT command set

…provides overviews of the supported sets of AT commands, separate for each type of command set.

…ts all the supported GSM 07.07 AT commands in alphabetical order, and indicates the type of … defined in the ETSI GSM 07.07 standard.

…mmand	Function	Type of command	Page
…M	Accumulated call meter	Mobile equipment control	33
…I	Alert sound mode	Mobile equipment control	33
…M	Accumulated call meter maximum	Mobile equipment control	34
…C	Advice of charge	Network service	18
	Battery charge	Mobile equipment control	34
…T	Select bearer service type	Modem command	65
…C	Call forwarding	Network service	19
…K	Clock	Mobile equipment control	34
…VA	Call waiting	Network service	20
…R	Query the reason for disconnection of last call	Call control	16
…ACT	PDP context activate or deactivate	GPRS	44
…ANS	Manual response to a network request for PDP context activation	GPRS	44
…ATT	GPRS attach or detach	GPRS	45
…AUTO	Auto response to a network request for PDP context activation	GPRS	45
…CLASS	GPRS mobile station class	GPRS	46
…DATA	Enter data state	GPRS	46
…DCONT	Define PDP Context	GPRS	47
…EREP	GPRS event reporting	GPRS	48
…MI	Issue manufacturer ID code	General	14
…MM	Issue model ID code	General	14
…MR	Output the GSM telephone version	General	14
…PADDR	Show PDP address	GPRS	51
…QMIN	Quality of Service Profile (Minimum acceptable)	GPRS	49
…QREQ	Quality of Service Profile (Requested)	GPRS	50
…REG	GPRS network registration status	GPRS	52
…SMS	Select service for MO SMS messages	GPRS	53
…SN	Output the serial number (IMEI)	General	14
…HLD	Call hold and multiparty	Network service	21
…HUP	Terminate call	Call control	16
…IMI	Output of IMSI	General	15
…KPD	Keypad control	General	15
…LCC	List Current Calls	Network service	22
…LCK	Switch locking on and off	Network service	23
…LIP	Display telephone number of calling party	Network service	24
…LIR	Select Incognito Mode (Call Line Identification	Call control	25

	Restriction)		
AT+CLVL	Loudspeaker volume level	Mobile equipment control	34
AT+CMEE	Expanded error messages according to GSM 07.07	Mobile equipment error	53
AT+CMUT	Mute control	Mobile equipment control	35
AT+COLP	Connected Line Identification Presentation	Call control	27
AT+COPN	Read operator names	Network service	27
AT+COPS	Commands concerning selection of network operator	Network service	28
AT+CPAS	Query the telephone status	Mobile equipment control	35
AT+CPBR	Read a telephone-book entry	Mobile equipment control	36
AT+CPBS	Select a telephone book	Mobile equipment control	37
AT+CPBW	Write a telephone-book entry	Mobile equipment control	38
AT+CPIN	Enter PIN and query lock	Mobile equipment control	39
AT+CPOL	Preferred operator list	Network service	29
AT+CPUC	Price per unit and currency table	Mobile equipment control	40
AT+CPWD	Change password to a lock	Network service	30
AT+CR	Service reporting control	General	16
AT+CRC	Cellular result codes	General	17
AT+CREG	Network registration	Network service	31
AT+CRLP	Select radio link protocol parameter for originating non-transparent data call	Modem command	66
AT+CRSL	Ringer sound level	Mobile equipment control	40
AT+CRSM	Restricted SIM access	Mobile equipment control	41
AT+CSCS	Select TE character set	General	15
AT+CSQ	Output signal quality	Mobile equipment control	42
AT+CSSN	Supplementary service notifications	Network service	32
AT+CVIB	Vibrator mode	Mobile equipment control	42
AT+GSN	Output the serial number (IMEI)	General	16
AT+VTS	Send a DTMF tone	TIA IS101	54
AT+VTD	Set duration of a DTMF tone	TIA IS101	54
AT+WS46	Select wireless network	General	16

Table 2-1: Supported GSM 07.07 commands

supported GSM 07.05 AT commands in alphabetical order, and indicates the type of
to the ETSI GSM 07.05 standard.

Function	Type of command	Page
Send an SMS command	Message sending and writing	55
Delete an SMS in the SMS memory	Message sending and writing	55
SMS format	General configuration	55
List SMS	Message receiving and reading	56
Read in an SMS	Message receiving and reading	56
Send an SMS	Message sending and writing	57
Write an SMS to the SMS memory	Message sending and writing	57
Send an SMS from the SMS memory	Message sending and writing	58
Acknowledgment of a short message directly output	Message receiving and reading	58
Display new incoming SMS	Message receiving and reading	60
Preferred SMS message storage	General configuration	62
Address of the SMS service center	Message configuration	63
Select cell broadcast messages	Message configuration	63
Selection of message service	General configuration	64

ted GSM 07.05 commands

e supported Siemens specific AT commands in alphabetical oder

Function	Page
quest Capabilities List	60
ed DTE rate	61

red commands according to ITU-T Recommendation V.25 ter

Table 2-3 lists all the supported AT commands for FAX services in alphabetical oder

Command	Function	Page
AT+ FBADLIN	Define or read number of bad lines	67
AT+ FBADMUL	Define, read or test number of bad lines	68
AT+ FBOR	Query the bit order for receive mode	68
AT+FCIG	Query or set the Local polling id	69
AT+FCLASS	Select, read or test FAX service class	70
AT+FCQ	Control Copy Quality	69
AT+ FCR	Capability to receive	70
AT+FDCC	Select service for MO SMS messages	71
AT+FDFFC	Data Compresssion Format Conversion	72
AT+FDIS	Query or set session parameters	73
AT+FDR	Begin or continue phase C data reception	74
AT+FDT	Data Transmission	75
AT+FET	End a page or document	75
AT+FK	Kill operation, orderly FAX abort	76
AT+FLID	Query or set session parameters	76
AT+FMDL	Identify Product Model	76
AT+FMFR	Request Manufacturer Identification	77
AT+FOPT	Set bit order independently	77
AT+FPHCTO	DTE Phase C Response Timeout	77
AT+FREV	Identify Product Revision	78
AT+FRH	Receive Data Using HDLC Framing	78
AT+FRM	Receive Data	78
AT+FRS	Receive Silence	79
AT+FTH	Transmit Data Using HDLC Framing	79
AT+FTM	Transmit Data	79
AT+FTS	Stop Transmission and Wait	80
AT+FVRFC	Vertical resolution format conversion	Fehler! Textmarke nicht definiert.

Table 2-4: Supported commands according to ITU-T Recommendation V.25 ter

s all the supported Siemens specific AT commands in alphabetical oder

nd	Function	Page
	Output ACM (accumulated call meter) and ACMmax	62
	Binary Read	63
V	Binary Write	64
	Output card ID	65
	Output SIM card status	65
	Output call number information	65
R	Database Read	66
D	Delete the "last number redial" memory	66
UTH	Select Type of Authentication for PPP connection	67
	Icon control	67
K	Switch locks (including user-defined locks) on and off	68
G	Language settings	69
O	SMS overflow indicator	90
L	List SMS (without status change from *unread* to *read*)	89
R	Read SMS (without status change from *unread* to *read*)	90
O	Switch device off	91
S	Select NF hardware	91
V	Set the volume	91
C	Seek the first entry in the sorted telephone book which begins with the selected (or next available) letter	92
G	Read entry from the sorted telephone book via the sorted index	92
S	Select a telephone book (including Siemens-specific books)	93
C	Output PIN counter	93
M	Read the PLMN	94
R	Read an entry from the preferred-operator	94
W	Write an entry to the preferred-operator	94
T	Play Signal Tone	95
WD	Change password to a lock (including user-defined locks)	95
TC	Set the ringing tone	96
TK	SIM Toolkit	96

6: Supported Siemens-specific commands

2.2 The AT command set

GSM mobile telephones and modems can be operated via Remote Control using a serial interface (data cable or infrared connection). Remote control is implemented by means of AT+C commands according to the ETSI GSM 07.07 [1] and GSM 07.05 [2] specifications, as well as several manufacturer-specific AT commands. These commands are described in more detail in section 2.3.2.

A command entered at the user port generally begins with an 'AT' command prefix. The remainder of the line is interpreted as a sequence of the commands described below. The commands are not case-sensitive. More than one command may be given on a single line, with the semicolon serving as the delimiter between commands.

The "ITU-T Draft new Recommendations V.25ter" specification [3] applies to the sequence of the interface commands. According to this guideline, commands should begin with the character string "AT" and end with "<CR>" (= 0x0D). The input of a command is acknowledged by the display of "OK" or "ERROR".

A command currently in process is interrupted by each additional character entered. This means that you should not enter the next command until you have received the acknowledgment, otherwise the current command is interrupted.

The commands supported are listed in the tables provided in sections 2.2.1 and 2.3.1 through 2.3.9.15.

2.2.1 Hayes Standard commands

The Hayes standard commands correspond to the commands of AT Hayes compatible modems.

All commands in Table 2-6 expect a numeric argument; if this argument is omitted, the default of 0 is assumed. **The ATD** command is a special command in that all characters specified in the same line (or up to a semicolon) are considered part of the number to dial.

Command	Function
A/	Repeat preceding command
AT	Prefix for all other commands
ATA	Accept call (V.25ter, according to [3])
ATB[n]	This modem command is used to set the bearer service for data connections (cf. AT+CBST) <n> can take one of the following values 7 2400bps, asynchronous, V.22bis 11 4800bps, asynchronous, V.32 13 9600bps, asynchronous, 32 15 14400bps, asynchronous, V.34 25 2400bps, asynchronous, V.110 ISDN 27 4800bps, asynchronous, V.110 ISDN 29 9600bps, asynchronous, V.110 ISDN 31 14400bps, asynchronous, V.110 ISDN

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Voltage, nt Darlington Arrays

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OCTAL PERIPHERAL
DRIVER ARRAYS

SEMICONDUCTOR
TECHNICAL DATA

ton connected transistors in this family of arrays acing between low logic level digital circuitry (such IOS/NMOS) and the higher current/voltage lays, printer hammers or other similar loads for a industrial, and consumer applications. All devices tputs and free wheeling clamp diodes for transient

gned to be compatible with standard TTL families mized for 6 to 15 volt high level CMOS or PMOS

A SUFFIX
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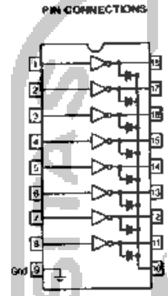
CASE 707

A = 25°C and rating apply to any one device in the noted.)

	Symbol	Value	Unit
	V_O	50	V
N2804)	V_I	30	V
nuous	I_C	500	mA
nt	I_B	25	mA
erature Range	T_A	0 to +70	°C
nge	T_{stg}	-55 to +150	°C
	T_J	125	°C

vrent limit per device

PIN CONNECTIONS



ORDERING INFORMATION

Characteristics		
Input Compatibility	$V_{CE}(Max)/I_C(Max)$	Operating Temperature Range
V CMOS, CMOS, PMOS	50 V/500 mA	T_A = 0 to +70°C

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ULN2803 ULN2804

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1)		I_{CEX}				µA
(V_O = 50 V, T_A = +70°C)	All Types			–	100	
(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802				500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804		–	.	500	
Collector-Emitter Saturation Voltage (Figure 2)		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)	All Types		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)	All Types		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)	All Types			0.85	1.1	
Input Current – On Condition (Figure 4)		$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802		–	0.82	1.25	
(V_I = 3.85 V)	ULN2803			0.93	1.35	
(V_I = 5.0 V)	ULN2804			0.35	0.5	
(V_I = 12 V)	ULN2804			1.0	1.45	
Input Voltage – On Condition (Figure 5)		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802		.	..	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803		–	.	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803			.	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803			..	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804		–		5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804		–		6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804		–		7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804		.	.	8.0	
Input Current – Off Condition (Figure 3) (I_C = 500 µA, T_A = +70°C)	All Types	$I_{I(off)}$	50	100	.	µA
DC Current Gain (Figure 2) (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	h_{FE}	1000	–	–	.
Input Capacitance		C_I	–	15	25	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}		0.25	1.0	µs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}		0.25	1.0	µs
Clamp Diode Leakage Current (Figure 6) (V_R = 50 V)	T_A = +25°C T_A = +70°C	I_R		–	50 100	µA
Clamp Diode Forward Voltage (Figure 7) (I_F = 350 mA)		V_F		1.5	2.0	V

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TEST FIGURES

(See Figure Numbers in Electrical Characteristics Table)

Figure 1.

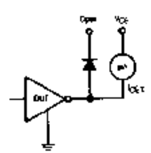


Figure 2.

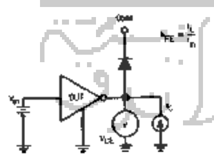


Figure 3.

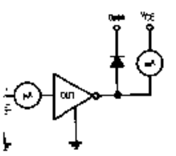


Figure 4.

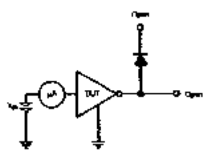


Figure 5.

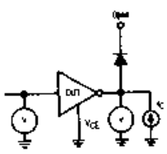


Figure 6.

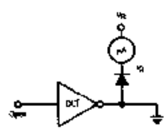
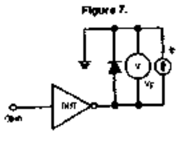


Figure 7.



ULN2803 ULN2804

TYPICAL CHARACTERISTIC CURVES – T_A = 25°C, unless otherwise noted

Output Characteristics

Figure 8. Output Current versus Saturation Voltage

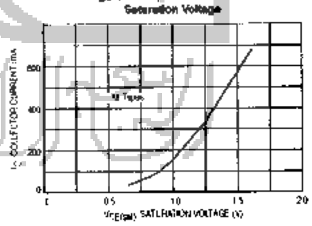
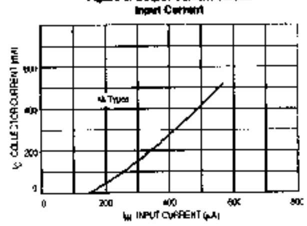


Figure 9. Output Current versus Input Current



Input Characteristics

Figure 10. ULN2803 Input Current versus Input Voltage

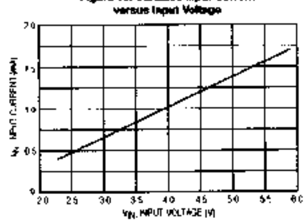


Figure 11. ULN2804 Input Current versus Input Voltage

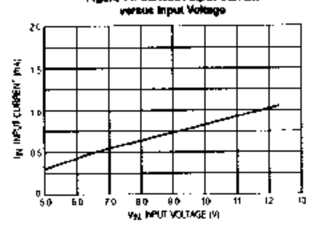
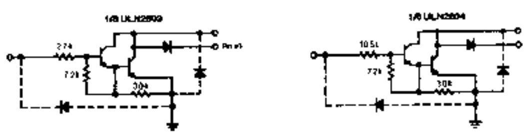


Figure 12. Representative Schematic Diagrams



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OUTLINE DIMENSIONS

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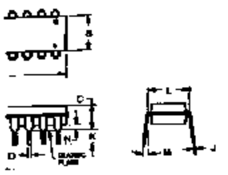

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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